

**REMARKS**

Claims 17-23, 25, 46-49 and 51-59 were pending in the present application.

Claims 17-23, 25, 58 and 59 are withdrawn from consideration.

Claims 46-49 and 51-57 are rejected.

Claim 46 was amended herein amended.

Claims 17-23, 25, 46-49 and 51-59 remain pending in the present application.

Reconsideration of the claims is respectfully requested.

**I. CLAIM REJECTION UNDER 35 U.S.C. §102**

Claims 46, 48, 49, 51, 52, 54 and 55 were rejected under 35 U.S.C. § 102(b) as being anticipated by “Fabrication Technique for Fully Recessed Oxide Isolation”, IBM Technical Disclosure Bulletin, March 1, 1977, Volume No. 19, Issue No. 10, page 3947-3950, hereinafter, “*IBM TDB*”. This rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131, p. 2100-67 (8<sup>th</sup> ed., rev. 5, August 2006) (*citing In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. *Id.* (*citing Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987)).

Claim 46 of the present application currently requires:

An integrated circuit device comprising:

- a substrate;
- a gate structure, wherein the gate structure includes:
  - a gate oxide layer on the substrate,
  - a nitride layer on and directly contacting the gate oxide layer, and
  - a polysilicon layer over the nitride layer;
- a channel region under the gate structure; and
- source/drain regions in the substrate adjacent the channel region,

wherein the gate structure has a peripheral edge and further including an uplift in portions of the nitride layer proximate the peripheral edge of the gate structure, the uplift caused by reoxidation of the polysilicon layer within the gate structure, *wherein asperities are absent from a bottom surface of the polysilicon layer and a thickness of an oxidation layer produced by said reoxidation is from about 25 Å to about 500 Å on said substrate.* (emphasis added).

Notably, Claim 46 requires a gate structure that has a peripheral edge and further including an uplift in portions of the nitride layer proximate the peripheral edge of the gate structure. The uplift is caused by reoxidation of the polysilicon layer within the gate structure. Importantly, asperities are absent from a bottom surface of the polysilicon layer and a thickness of an oxidation layer produced by said reoxidation is from about 25Å to about 500Å on said substrate.

*IBM TDB*, on the other hand, fails to teach anything about asperities, let alone teach or disclose that *asperities are absent from a bottom surface of polysilicon layer* after reoxidation, as required by Claim 46. In fact, *IBM TDB* fails to teach anything about *reoxidation of the gate structure* that would result in the prevention (let alone elimination) of *asperities* on the *bottom surface of the polysilicon layer*, as currently required by Claim 46. In addition, *IBM TDB* also fails to teach or disclose anything about the thickness of the oxidation layer *produced by reoxidation*, as also currently required by Claim 46.

Claim 46 and its dependents, Claims 48, 49, 51, 52, 54 and 55, are thus allowable. Accordingly, the Applicants respectfully request favorable reconsideration and the withdrawal of §102 rejection.

## II. CLAIM REJECTION UNDER 35 U.S.C. §103

Claims 46-49, 52, 53 and 55-57 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,192, 059 to *Khan, et al.*, hereinafter “*Khan*” and in view of the *IBM TDB* reference. This rejection is respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142, p. 2100-125 (8th ed. rev. 5, August 2006). Absent such a *prima facie* case, the applicant is under no obligation to produce evidence of nonobviousness. *Id.* To establish a *prima facie* case of obviousness, three basic criteria must be met: *Id.* First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. *Id.* Second, there must be a reasonable expectation of success. *Id.* Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *Id.* The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant’s disclosure. *Id.*

Again, *IBM TDB*, fails to teach anything about asperities, let alone teach or disclose that *asperities are absent from a bottom surface of polysilicon layer* after reoxidation, as required by

Claim 46. In fact, *IBM TDB* fails to teach anything about *reoxidation of the gate structure* that would result in the prevention (let alone elimination) of *asperities* on the *bottom surface of the polysilicon layer*, as currently required by Claim 46. In addition, *IBM TDB* also fails to teach or disclose anything about the thickness of the oxidation layer *produced by reoxidation*, as also currently required by Claim 46. *Khan* fails to cure these deficiencies.

*IBM TDB*, either alone or in any combination with *Khan*, therefore fails to teach or disclose every element of Claim 46. Moreover, there is no suggestion or motivation within either of these reference to prompt one of ordinary skill to selectively combine discrete elements from each and then seek out still others as required by Claim 46 and its dependents, Claims 47-49, 52, 53 and 55-57.

Accordingly, the Applicants respectfully request favorable reconsideration and the withdrawal of the §103 rejection.

**CONCLUSION**

As a result of the foregoing, the Applicants assert that the remaining claims in the Application are in condition for allowance, and respectfully requests that this Application be passed to issue.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *dvenglarik@munckbutrus.com*.

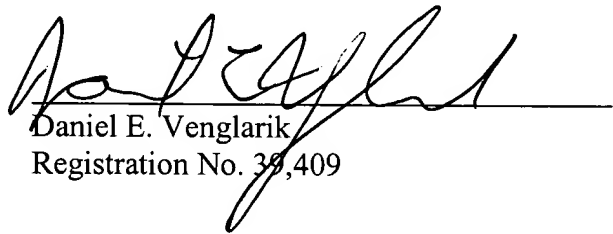
The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK BUTRUS, P.C.

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